

29. The method of claim 23, further comprising:  
forming a layer of metal on the substrate before forming the first layer of spin-on  
glass; and

forming the first layer of spin-on glass on the layer of metal.

30. The method of claim 23, further comprising:  
forming a layer of metal on the substrate before forming the first layer of spin-on  
glass;

depositing a second dielectric on the layer of metal before forming the first layer  
of spin-on glass; and

forming the first layer of spin-on glass on the second dielectric.

31. The method of claim 23 wherein depositing the first dielectric comprises  
performing a plasma-enhanced deposition of the first dielectric onto the first layer of  
spin-on glass.

32. The method of claim 23 wherein depositing the first dielectric comprises  
depositing an oxide onto the first layer of spin-on glass.

33. The method of claim 23 wherein depositing the first dielectric comprises  
depositing a low-temperature oxide onto the first layer of spin-on glass.

34. The method of claim 23, further comprising planarizing the first dielectric  
while planarizing the second layer of spin-on glass.

35. The method of claim 23, further comprising planarizing the first dielectric  
and the first layer of spin-on glass while planarizing the second layer of spin-on glass.

36. The method of claim 23 wherein planarizing the second layer of spin-on  
glass comprises etching back the second layer of spin-on glass.

37. The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric while etching back the second layer of spin-on glass.

38. The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric and the first layer of spin-on glass while etching back the second layer of spin-on glass.

39. A semiconductor structure, comprising:

a substrate;

a first layer of spin-on glass disposed on the substrate;

a first dielectric disposed on the first layer; and

a planarized second layer of spin-on glass disposed on the first dielectric.

40. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a siloxane-based spin-on glass.

41. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polyimide spin-on glass.

42. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polymethylmethacrylate spin-on glass.

43. The semiconductor structure of claim 39, further comprising:

a second dielectric disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the second dielectric.